WHAT IS CLAIMED IS:

1. A capacitor comprising a first conducting film formed on a substrate, a first dielectric film formed on the first conducting film, a second conducting film formed on the first dielectric film, a second dielectric film formed above the second conducting film, covering an edge of the second conducting film, and a third conducting film formed above the second dielectric film, covering a part of the second dielectric film covering the edge of the second conducting film,

the capacitor further comprising:

an insulation film covering said edge of the second conducting film or said part of the second dielectric film.

2. A capacitor according to claim 1, wherein

said edge has a step.

3. A capacitor according to claim 1, wherein

said edge is an inner edge of an opening formed in the second conducting film, or an outer edge of the second conducting film.

4. A capacitor according to claim 1, wherein

a total thickness of a thickness of the second dielectric film covering said edge and a thickness of the insulation film is larger than a thickness of the second dielectric film in a region other than said edge.

5. A capacitor according to claim 1, wherein

the first dielectric film and/or the second dielectric

film is formed of a material having a higher relative dielectric constant than silicon dioxide.

6. A capacitor according to claim 5, wherein

the first dielectric film and/or the second dielectric film is formed of a composite oxide containing at least one element of Sr, Ba, Pb, Zr, Bi, Ta, Ti, Mg and Nb.

7. A capacitor according to claim 6, wherein

the first dielectric film and/or the second dielectric film is formed of $(Ba,Sr)TiO_3$, $Pb(Zr,Ti)O_3$, $SrBi_2Ta_2O_9$, $Pb(Mg,Nb)O_3$ or Ta_2O_5.

8. A capacitor according claim 1, wherein

the insulation film is formed of a material having a higher voltage resistance than a material of the first dielectric film and/or the second dielectric film.

9. A capacitor according to claim 1, wherein

the insulation film is formed of a material having a higher relative dielectric constant than silicon dioxide.

10. A capacitor according to claim 9, wherein

the insulation film is formed of a composite oxide containing at least one element of Sr, Ba, Pb, Zr, Bi, Ta, Ti, Mg and Nb.

11. A capacitor according to claim 10, wherein

the insulation film is formed of $(Ba,Sr)TiO_3$, $Pb(Zr,Ti)O_3$, $SrBi_2Ta_2O_9$, $Pb(Mg,Nb)O_3$ or Ta_2O_5.

12. A capacitor according to claim 1, wherein

the insulation film is formed of polyimide.

13. A capacitor according to claim 1, wherein

the insulation film is formed of an inorganic substance.

14. A capacitor according to claim 1, wherein

the first conducting film, the second conducting film or the third conducting film is formed of Pt, Au, Cu, Pd, Ru, Ru oxide, Ir or Ir oxide.

15. A capacitor according to claim 1, wherein

the substrate is silicon substrate or glass substrate.

16. A semiconductor device comprising a capacitor, the capacitor comprising a first conducting film formed on a substrate, a first dielectric film formed on the first conducting film, a second conducting film formed on the first dielectric film, a second dielectric film formed above the second conducting film, covering an edge of the second conducting film, and a third conducting film formed above the second dielectric film, covering a part of the second dielectric film covering the edge of the second conducting film,

the capacitor further comprising:

an insulation film covering said edge of the second conducting film or said part of the second dielectric film.

17. A semiconductor device comprising:

a semiconductor element substrate;

a passive component mounted on the semiconductor element substrate and electrically connected to electrodes

of the semiconductor element substrate;

column-shaped conductors formed on the semiconductor element substrate in a region other than a region where the passive component is mounted, and having a height which is substantially flush with at least the upper surface of the passive component, and

an insulation layer burying the passive component and the column-shaped conductors,

the upper surfaces of the column-shaped conductors being exposed on the surface of the insulation film.

18. A semiconductor device comprising:

a semiconductor element substrate;

a passive component mounted on the semiconductor element substrate and electrically connected to electrodes of the semiconductor substrate;

column-shaped conductors formed on the semiconductor element substrate in a region other than a region where the passive component is mounted; and

an insulation layer burying the passive component and the column-shaped conductors,

the semiconductor element substrate being electrically connected to an outside terminal via the column-shaped conductors.

19. A semiconductor device according to claim 17, wherein

the passive component includes a passive element

formed on a side of a support substrate opposed to the semiconductor element substrate, and

the passive component includes electrodes electrically connected to the passive element and exposed on the side of the upper side of the support substrate.

20. A semiconductor device according to claim 19, wherein

the electrodes exposed on the side of the upper surface of the support substrate are electrically connected to the passive element through the support substrate.

21. A semiconductor device according to claim 17, wherein

a pitch of a plurality of the electrodes of the semiconductor element substrate is smaller than a pitch of a plurality of the column-shaped conductors.

22. A semiconductor device according to claim 19, wherein

the passive component further comprises through-electrodes insulated from the passive element and electrically connected to the semiconductor element substrate through the passive component.

23. A semiconductor device according to claim 17, wherein

the upper surface of the passive component is covered with the insulation layer.

24. A semiconductor device comprising a semiconductor

element substrate, and a passive component mounted on the semiconductor element substrate and electrically connected to electrodes of the semiconductor element substrate,

the passive component including a passive element formed on a side of a support substrate opposed to the semiconductor element substrate, and

the passive component including electrodes electrically connected to the passive element through the support substrate and exposed on the upper surface of the support substrate, and through-electrodes electrically connected to the semiconductor element substrate through the passive component and insulated from the passive element.

25. A semiconductor device comprising a semiconductor element substrate, and a passive component including a passive element mounted on the semiconductor element substrate and electrically connected to electrodes of the semiconductor element substrate,

the passive component including electrodes electrically connected to the passive element and exposed on the upper surface of the passive component, and through-electrodes electrically connected to the semiconductor element substrate through the passive component and insulated from the passive element.

26. A semiconductor device according to claim 22, further comprising:

a wiring layer formed on the semiconductor element substrate and having relay wiring,

the passive element, the column-shaped conductors or the through-electrodes are electrically connected to the semiconductor element substrate via the relay wiring.

27. A semiconductor device according to claim 24, further comprising:

a wiring layer formed on the semiconductor element substrate and having relay wiring,

the passive element, the column-shaped conductors or the through-electrodes are electrically connected to the semiconductor element substrate via the relay wiring.

28. A semiconductor device according to claim 25, further comprising:

a wiring layer formed on the semiconductor element substrate and having relay wiring,

the passive element, the column-shaped conductors or the through-electrodes are electrically connected to the semiconductor element substrate via the relay wiring.

29. A semiconductor device according to claim 17, wherein

the passive component is flip chip-bonded to the electrodes of the semiconductor element substrate or the electrodes formed on the wiring layer.

30. A semiconductor device according to claim 24, wherein

the passive component is flip chip-bonded to the electrodes of the semiconductor element substrate or the electrodes formed on the wiring layer.

31. A semiconductor device according to claim 25, wherein

the passive component is flip chip-bonded to the electrodes of the semiconductor element substrate or the electrodes formed on the wiring layer.

32. A semiconductor device according to claim 17, wherein

the passive component is a capacitor, a resistor, or an inductor.

33. A semiconductor device according to claim 24, wherein

the passive component is a capacitor, a resistor, or an inductor.

34. A semiconductor device according to claim 25, wherein

the passive component is a capacitor, a resistor, or an inductor.

35. A method for fabricating a semiconductor device comprising the steps of:

forming column-shaped conductors on a semiconductor element substrate;

mounting a passive component including a passive element formed on a side of a support substrate opposed to

the semiconductor element substrate, on the semiconductor element substrate in a region other than a region where the column-shaped conductors are formed;

forming an insulation layer, burying the column-shaped conductors and the passive component; and

polishing the side of the upper surface of the support substrate together with the insulation layer.

36. A method for fabricating a semiconductor device according to claim 35, wherein

the step of forming the column-shaped conductors includes the step of forming a conducting film on the semiconductor element substrate with a plurality of electrodes formed on the upper surface, the step of forming on the conducting film a mask with openings formed in; the step of forming by plating the column-shaped conductors on the conductor film in the openings; and the step of etching the conducing film in a region where the column-shaped conductors are not formed to electrically isolate said plural electrodes from each other.

37. A method for fabricating a semiconductor device comprising the steps of: mounting on a semiconductor element substrate a passive component including a passive element formed on a side of a support substrate opposed to the semiconductor element substrate, electrodes electrically connected to the passive element through the support substrate and exposed on the upper surface of the

support substrate, and through-electrodes passed through the support substrate and insulated from the passive element; and

polishing the side of the upper surface of the support substrate.